

AMENDMENT AND RESPONSE

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Serial Number: 09/145,595

Dkt: 303,537US1

Filing Date: September 2, 1998

Title: STRUCTURE AND METHOD FOR REDUCED EMITTER TIP TO GATE SPACING IN FIELD EMISSION DEVICES

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein

forming the gate insulator layer includes ion etching the insulator layer

such that the insulator layer is formed thinner around the emitter tips than

in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips, and

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate.

43. (Once Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes formed in rows along the substrate;

a gate insulator formed along the substrate and surrounding the cathodes;

a number of gate lines formed on the gate insulator; and

a number of anodes formed in columns orthogonal to and opposing the rows of cathodes, wherein the anodes include multiple phosphors, and wherein the intersection of the rows and columns form pixels, the field emitter array formed by a method comprising:

forming a number of cathode emitter tips in cathode regions of the substrate;

forming a gate insulator layer on the emitter tips and the substrate, wherein

forming the gate insulator layer includes ion etching the insulator

layer such that the insulator layer is formed thinner around the

emitter tips than in an isolation region of the substrate;

forming a number of gate lines on the gate insulator layer; and

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forming a number of anodes opposite the emitter tips;
wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate.

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on April 3, 2000, and the references cited therewith.

Claims 36 and 43 are amended. As a result, claims 36-46 are now pending in this application. Applicant respectfully requests reconsideration of the pending claims in view of the following remarks.

Rejections Under 35 U.S.C. §103

Claims 36-46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Cloud et al. (U.S. Patent No. 5,653,619). The rejection states in part,

Method limitations in claim 36 and claim 37 have not been given patentable weight since the method of forming the device is not germane to the issue of patentability of the device itself (see MPEP 2113).

Applicant acknowledges that,

[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). MPEP 2113.